



Long Term Perspective for Engine Embedded Electronics

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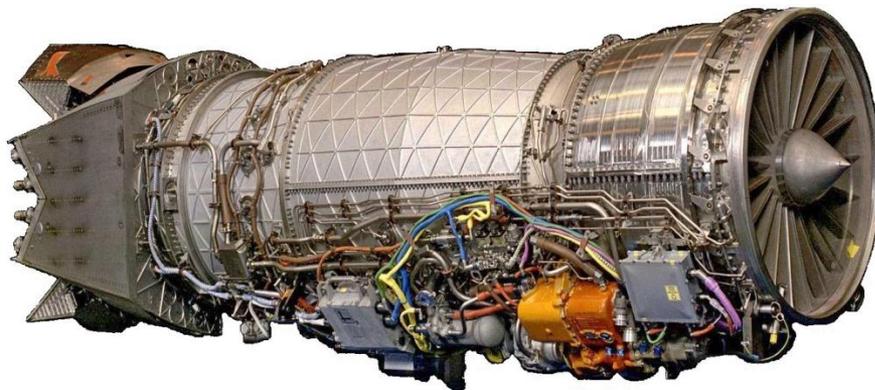
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High Temperature Electronics: An Enabler for Distributed Engine Control

Centralized control architecture with FADEC has been used since the mid 1980's

Distributed engine control features:

- Data concentrators
- Smart sensors/actuators
- Local loop closure
- Digital I/O
- Plug and play
- Sensor bus
- Reduced wire count and weight
- Increased reliability
- Expandability, flexibility, modularity



Credit: P&W public release

Implementation of distributed control inhibited by lack of high temperature electronics

- Active cooling of distributed modules is impractical
- Catalog of 225 °C silicon-on-insulator (SOI) electronics needed
- Use SiC for $T > 300$ °C
 - In-package sensor signal conditioning
 - Smart P3 sensor

Applications for High Temperature SiC Electronics

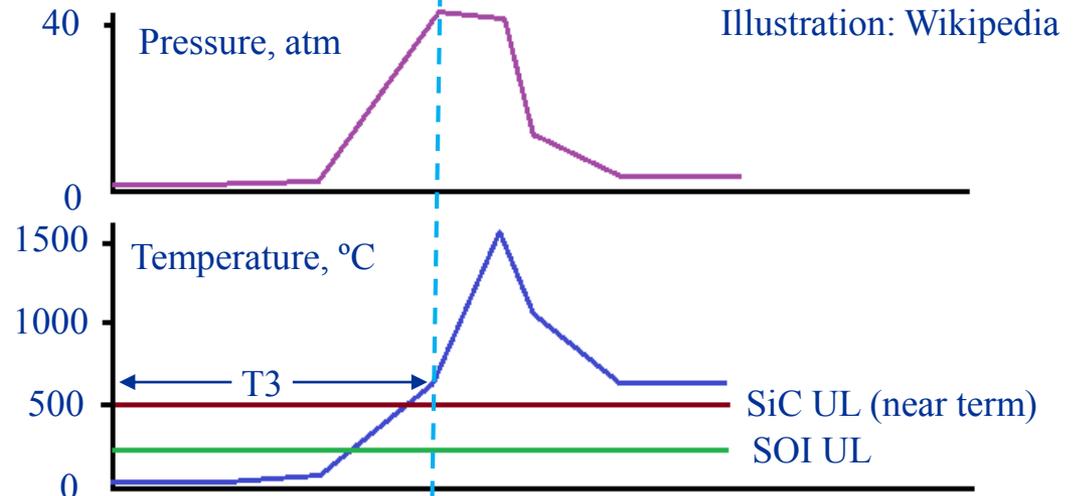
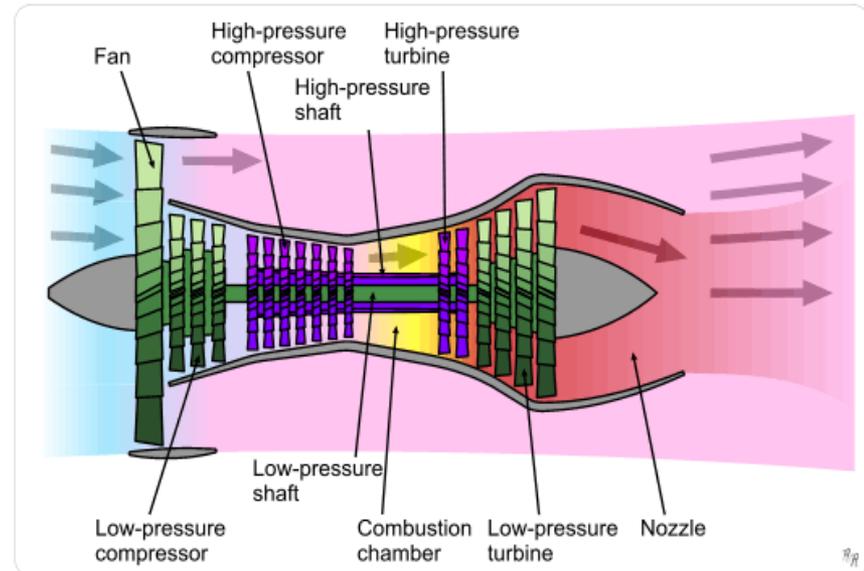
- 500 °C durable SiC electronics enable in-package sensor signal conditioning in hot regions of engine:
- **In gas path**; from inlet to last stages of compressor
- **In back end of sensor probe**; can use in more locations, including compressor discharge and front part of combustor

- Desirable to withstand compressor discharge temperature (T3):

P3/P1	T3
30	540 °C
40	615 °C
50	675 °C

(T1=59 °F, P1=1 atm, 90% comp. eff.)

- No fundamental reason SiC electronics cannot operate > 500 °C
- Recently we have demonstrated 10s of hrs of operation of our SiC electronics at 727 °C (failed die attach)



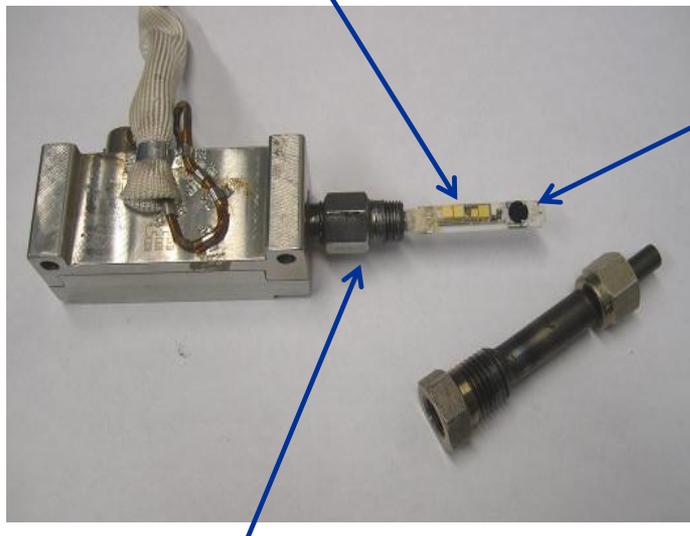
Core gas path pressures and temperatures for 42:1 pressure ratio engine

SiC Electronics Application: Smart P3 Sensor

An SiC or SiCN pressure sensor with in-package SiC signal conditioning electronics to provide both dynamic and low frequency pressure measurements at the compressor discharge

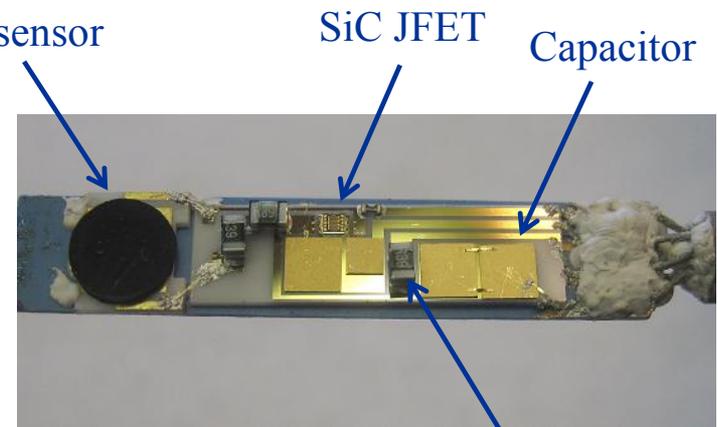
- Use existing port
- Dynamic P3 measurements can enable determination of stall margin
- Margin can then be safely reduced to enhance performance
- In-package signal conditioning electronics essential for capacitive sensors and for detection of low level dynamic signals using piezoresistive pressure sensors
- Distributed control architecture enables active stall margin control (using SOI controller)

Oscillator circuit using SiC JFET



Pressure feedthrough

SiCN capacitive pressure sensor



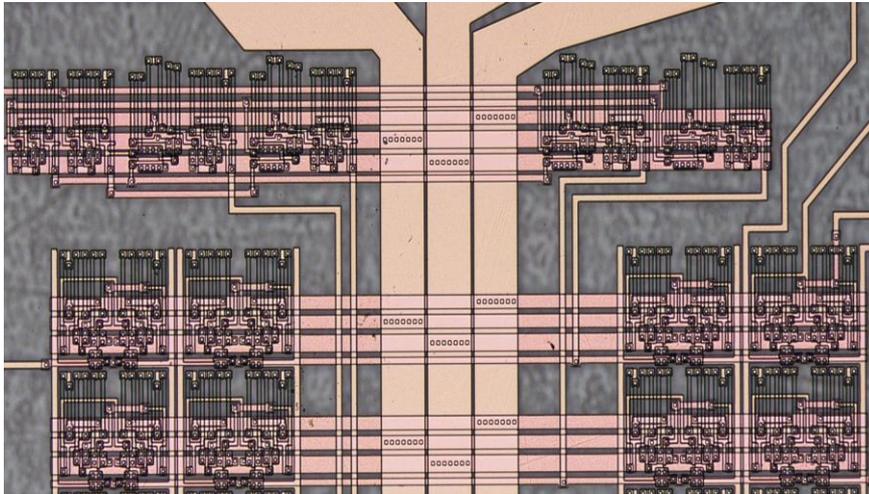
Resistor

High temperature capacitive pressure sensor tested on F117 compressor in VIPR-3

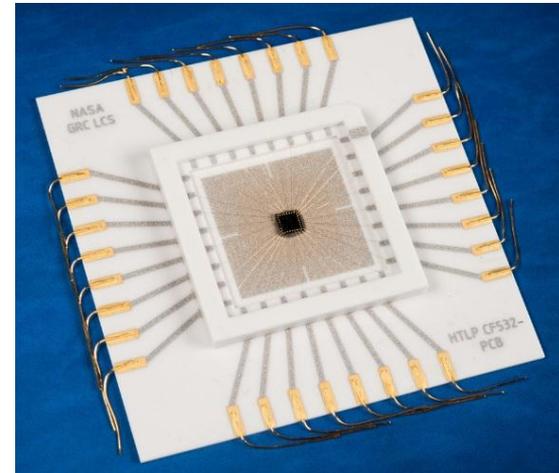
Credit: Max Scardelletti (GRC); Kevin Harsh, Evan Pilant, Mike Usrey (Sporian)

SiC High Temperature Electronics Status

- Simple SiC ICs (<10 transistors) demonstrated at 500 °C for 1000s of hrs in 2007
- Since then, we've been working to increase complexity of these high temperature ICs
- Multilevel interconnect system (i.e., circuit traces cross over one another) needed to increase transistor count to 100s or 1000s per IC
- First wafer of SiC ICs using multilevel interconnect fabricated in 2015
 - Circuits for high temperature smart sensors (e.g., op amp, A/D, memory)
 - 3000 hrs of 500 °C operation demonstrated for 10 transistor ring oscillator circuit
 - Issues uncovered, fixes being implemented



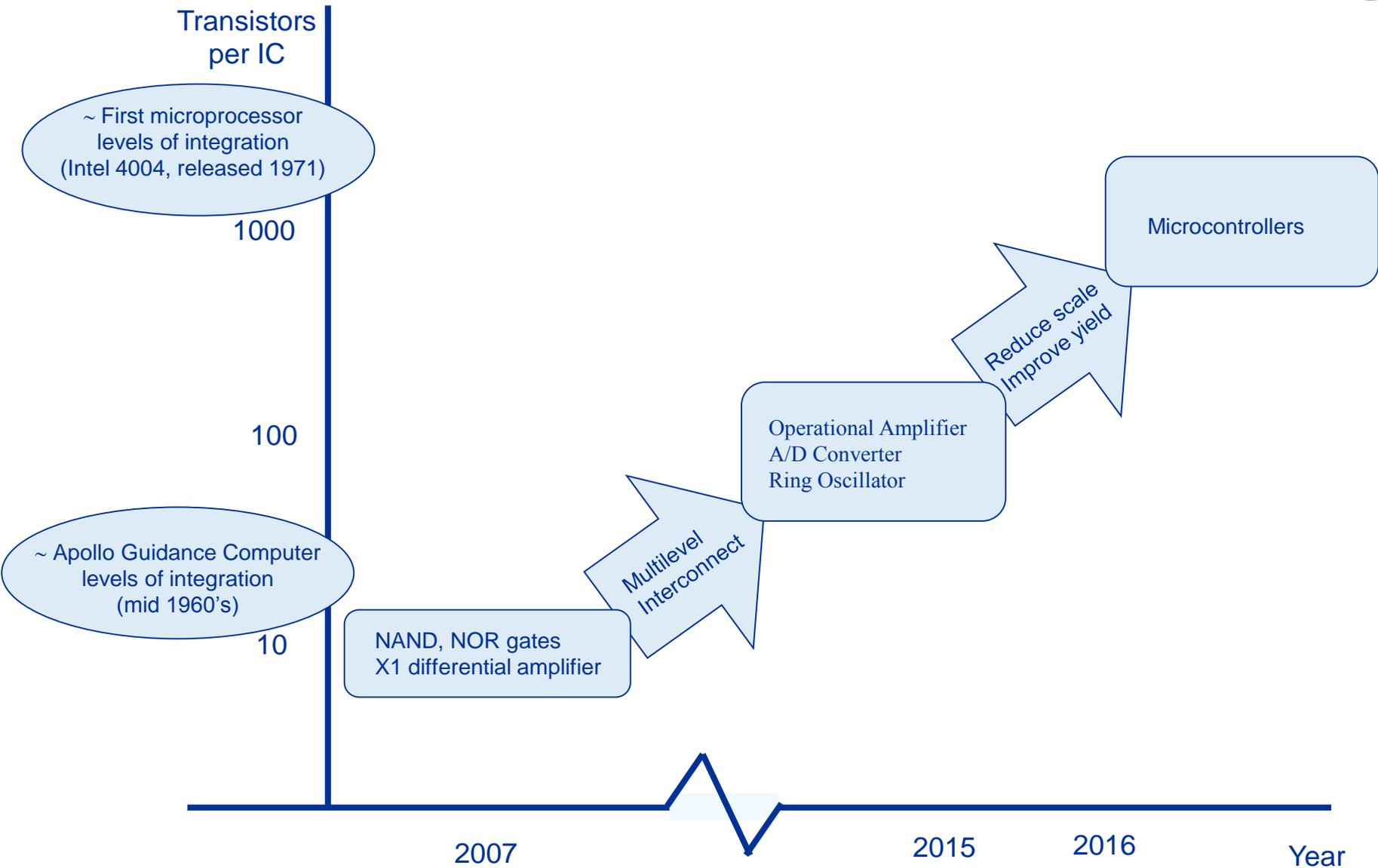
Portion of 4 X 4-Bit random access memory (RAM)
containing 220 transistors



Packaged SiC die mounted on circuit
board for long term high temperature
testing



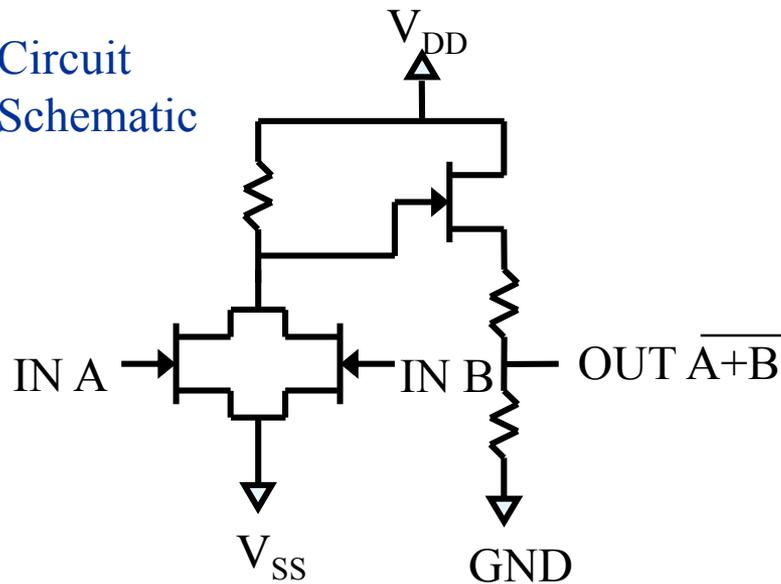
Development of High-Temperature SiC Integrated Circuits



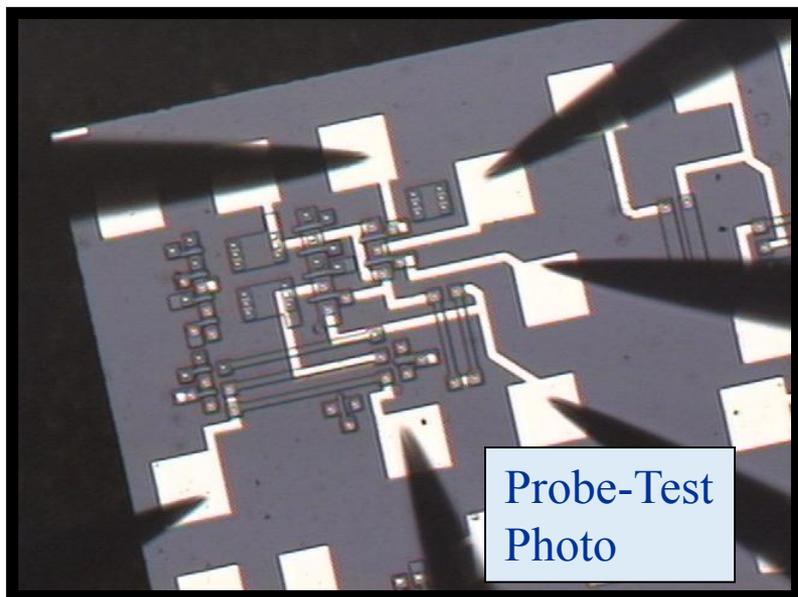
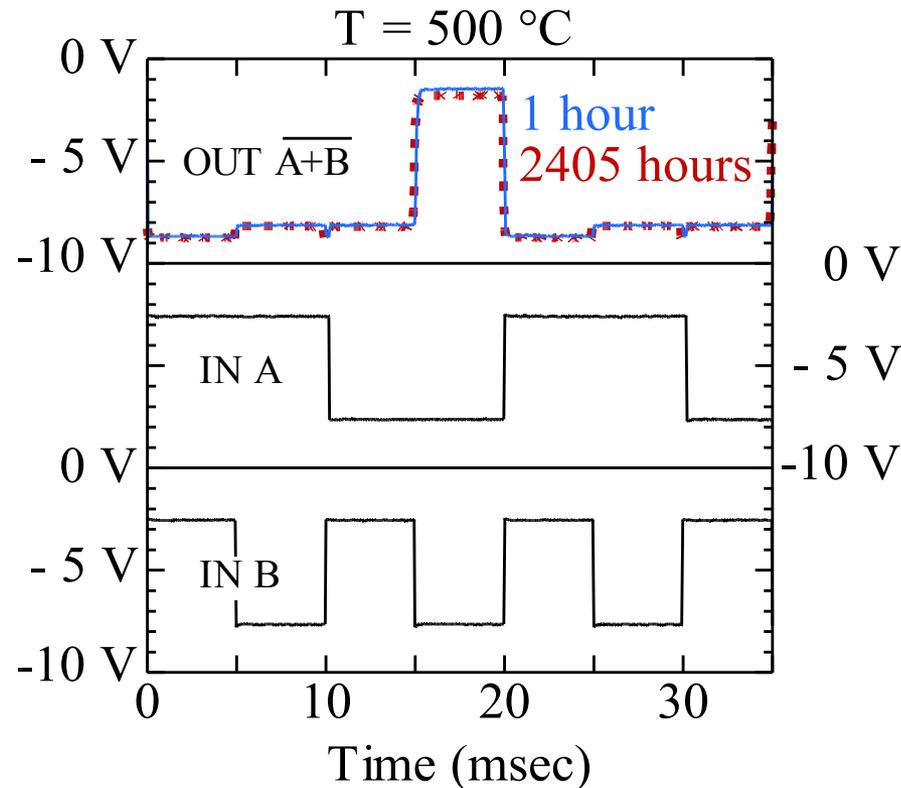
Single-Level Interconnect Digital Devices (2007): NOR gate

World's First Semiconductor Digital IC to Surpass 2000 hours of 500 °C Operation

Circuit
Schematic



Waveforms of **packaged** NOR gate

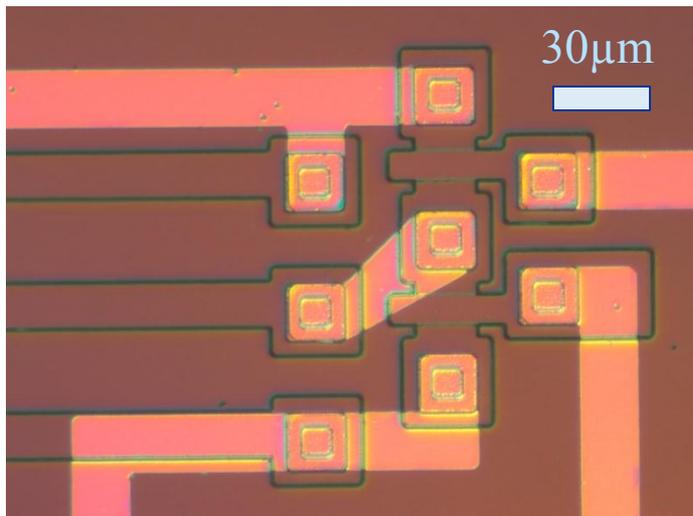


- Digital IC failures between 2000 & 4000 hours
- Higher supply voltages than analog circuits
 - Interconnect/insulator failure

Single-Level Interconnect Analog Devices (2007): Differential Amplifier

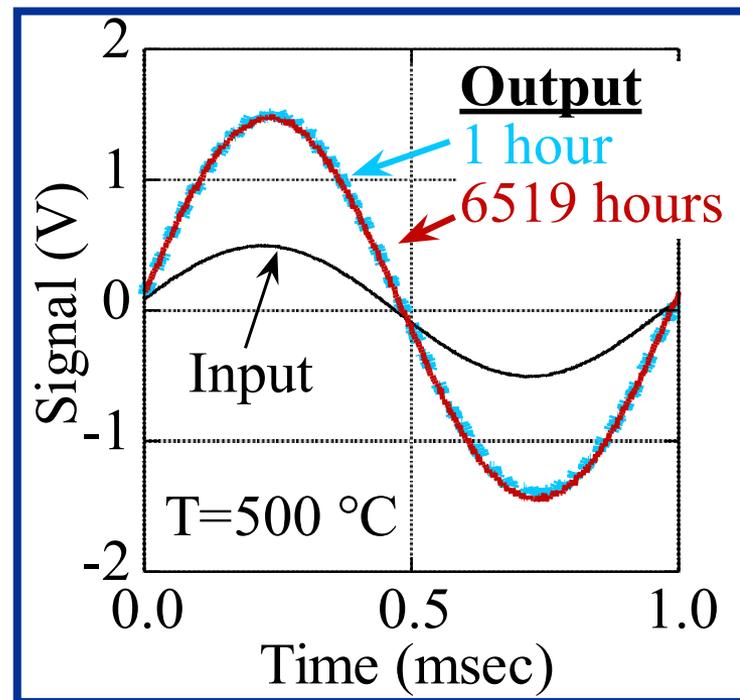
World's First Semiconductor IC to Surpass
6000 Hours of Electrical Operation at 500 °C

Optical micrograph of demonstration
amplifier circuit before packaging



2 transistors and 3 resistors integrated
into less than half a square
millimeter.

Amplifier test voltage waveforms

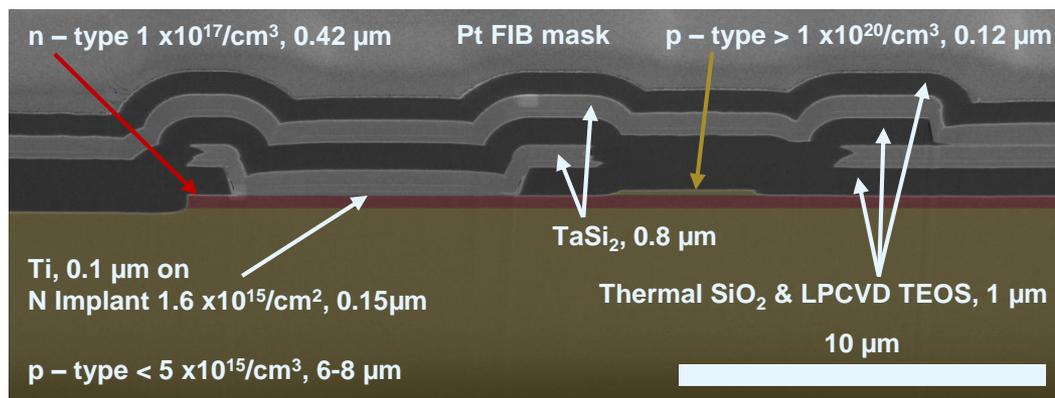


Less than 5% change in
operating characteristics during 6500
hours of 500 °C operation.

Multilevel Interconnect

Why so difficult?

- High aspect ratio surface topography
 - SiC mesa etches, thick SiO₂ insulating and TaSi₂ conducting layers
 - Dictated by operating environment, e.g., insulator quality is reduced at high temperature, therefore thicker layers are needed
 - Physical vapor deposition of TaSi₂ tends to yield nonuniform density and thickness on a surface with topography (typical for high melting point materials)
 - Remedied by extremely close range sputtering technique
- High stresses caused by mismatched thermal expansion coefficients (Pt vs. SiO₂) and wide temperature range, 20 °C to 500 °C (testing) and 720 °C (during processing)
 - Design changed to accommodate stresses without peeling, SiO₂ cracking

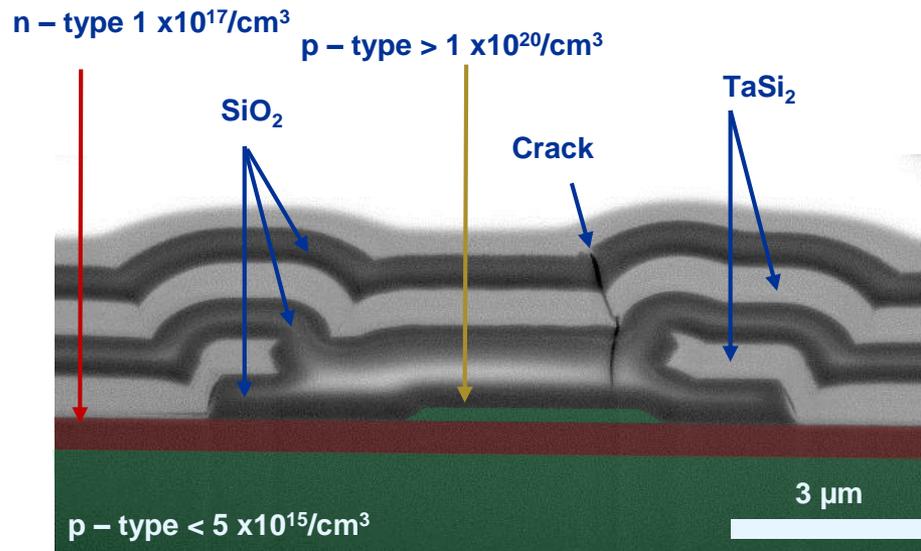


Cross sectional SEM image of 4H SiC JFET and two layer interconnect. The false color red and green shading was added to show the doped SiC layers.

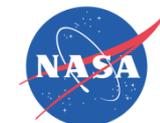
Multilevel Interconnect

Process and Design Improvements

- Close-range sputter deposition of conformal uniformly dense layers of TaSi_2
- Low pressure chemical vapor deposited (LPCVD) SiO_2 and Si_3N_4
- New metal-SiC contacts compatible with multilevel interconnect processing
- New bond pad structure prevents insulator cracking because of thermally induced stress
- Increased repeatability and yield of process steps



Issue: cracks sometimes observed where metal 1 and metal 2 overlaps the gate (mask misalignment). Design changes have mitigated this problem.



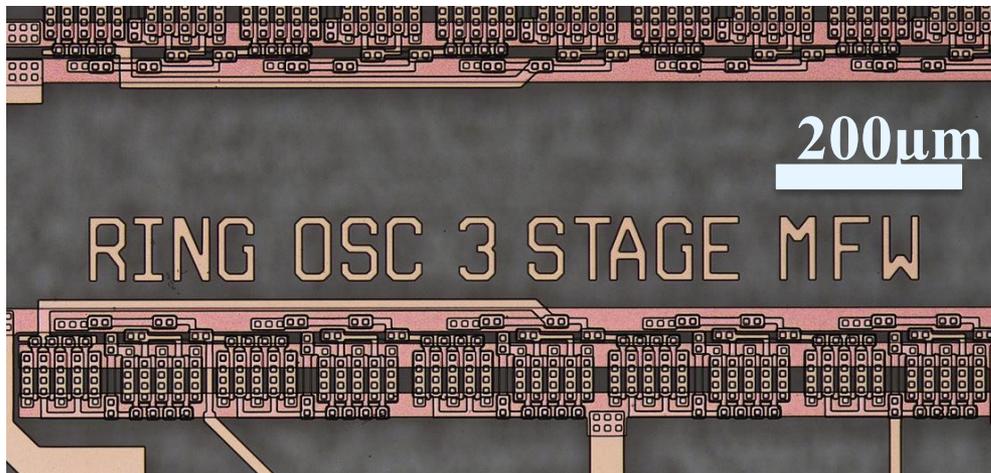
Multilevel Interconnect Wafer ICs

Circuit	Inputs	Outputs	Transistors, I/O Pads	Comments
4-Bit A/D	Analog voltage signal, optional external clock, output type select	4 bit parallel digital latch, pulse width modulated (PWM)	203 JFETs, 23 I/Os	Internal ring-oscillator clock circuit
4X4 Bit Static RAM	Read, Write, Data Lines, Address Lines	4 bit parallel digital latch, pulse width modulated (PWM)	220 JFETs, 30 I/Os	Address decoder, sense amplifiers
Source Separation Sensor Signal Transmitter	Capacitive sensor	Frequency modulated with address code	301 JFETs, 20 I/Os	Each sensor signal is tagged with unique address code
Ring Oscillators	Capacitive sensors	Frequency modulated signals (up to 500 MHz)	10-12 JFETs, 6 I/Os	On-chip large transistors for power amplification
Binary Amplitude Modulation RF Transmitter	Low power binary signal	High-Power RF signal to antenna		Could connect with PWM from A/D
Op Amp, 2-Stage	Differential	Voltage gains to 50 w/ on-chip resistors	10 JFETs	For piezoelectric SiC pressure sensors
4-Bit D/A	4 digital	1 analog	20 JFETs	

Ring Oscillator

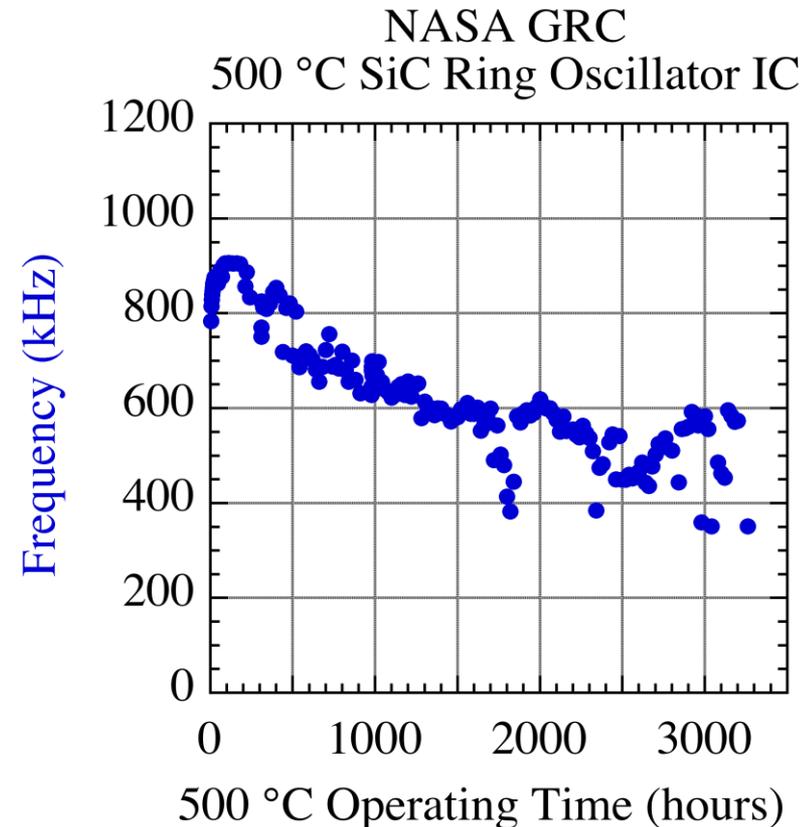
- In-package signal conditioning for capacitive pressure sensors
- Change in capacitance modifies the oscillation frequency
- Provides frequency coded pressure measurement

10-Transistor Ring Oscillator IC



World-First Demonstration of Multi-Level Interconnect Integrated Circuit With Prolonged 500 °C Operation

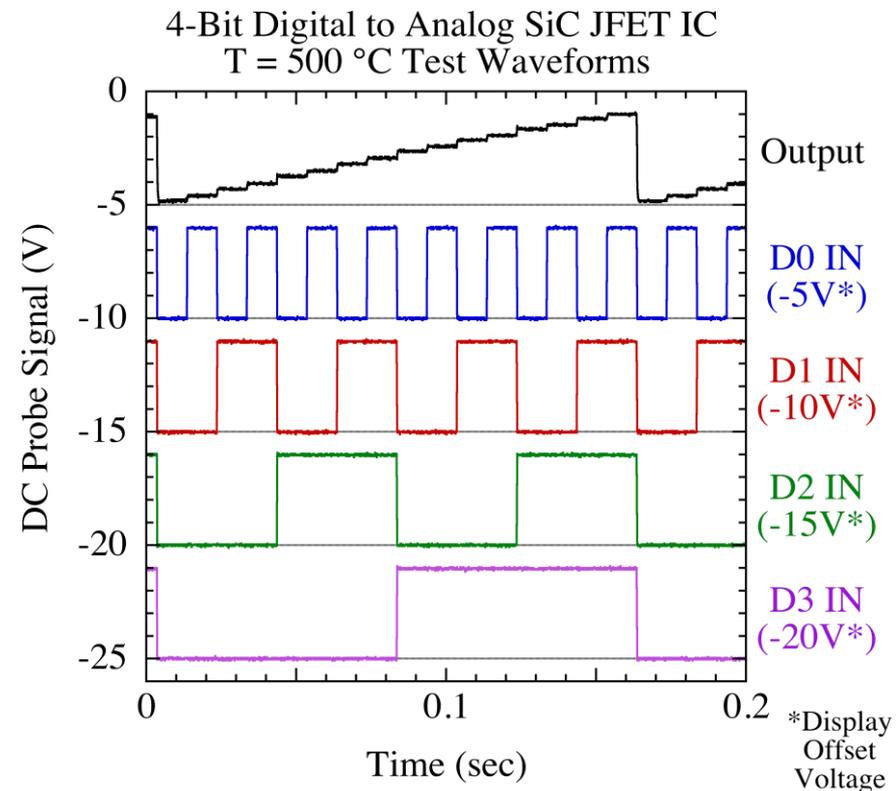
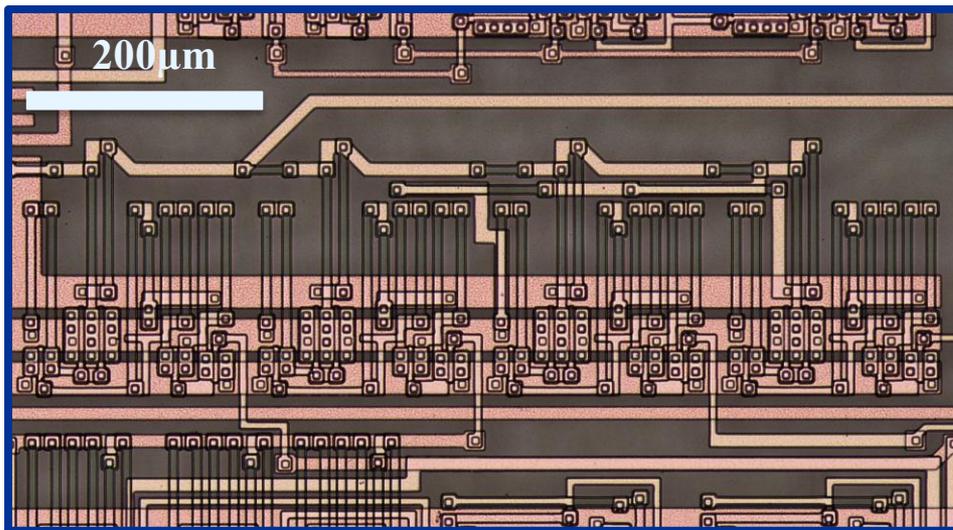
Power supply biases were adjusted during prolonged testing to keep circuit functioning. 500 °C testing was concluded with circuit failure around 3200 hours.



Digital to Analog (D/A) Converter

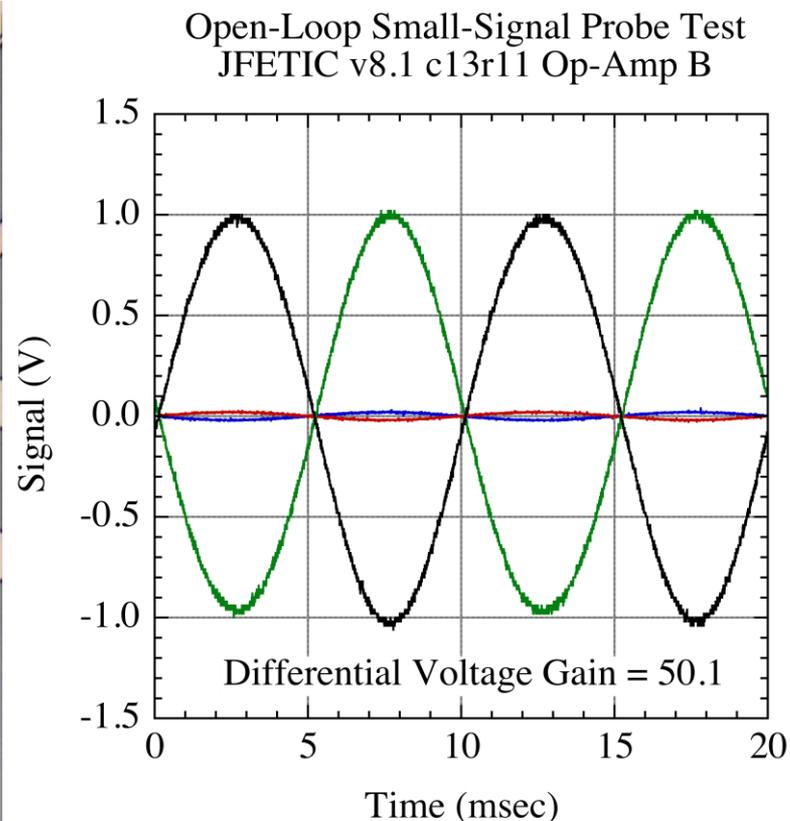
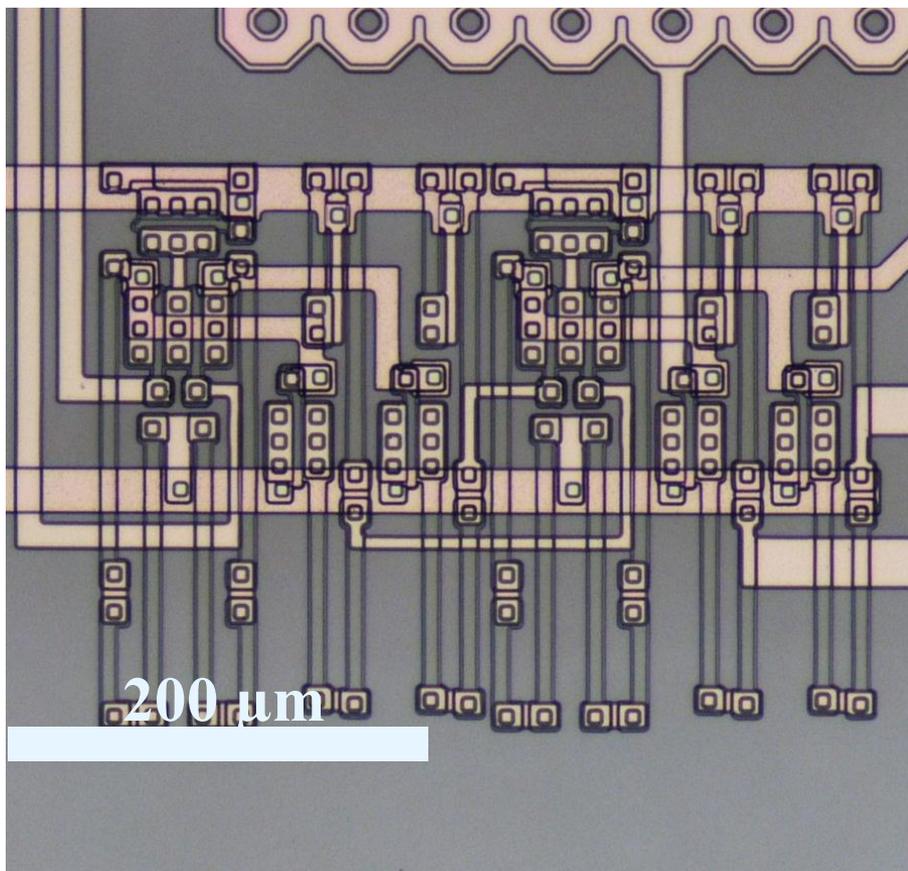
- D/A is a component of an A/D converter (A/D did not work because of design error)
- A/D can provide in-package digitization of sensor
- Future versions to provide higher bit count

4-Bit Digital to Analog Integrated Circuit (16 SiC JFETs)



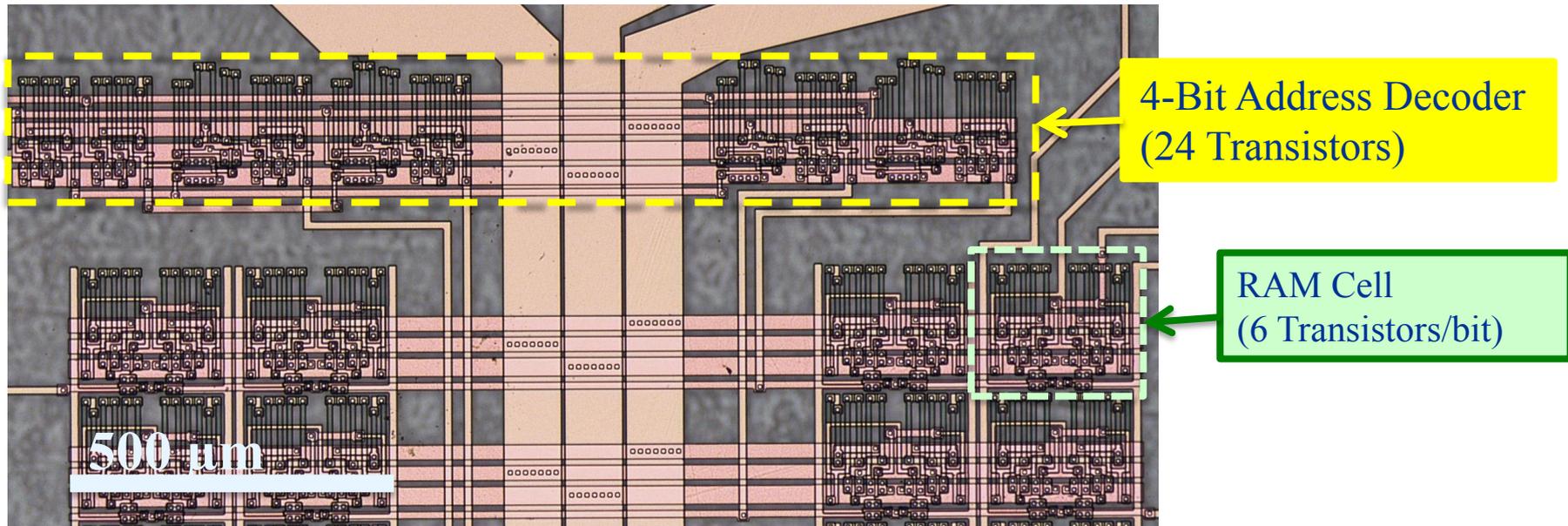
Operational Amplifier

- Analog building block. Provides amplification of low level sensor signal.
- Op amps work at room temperature
- Do not work at high temperature because of mobile ion contamination; we are implementing process improvements to correct this in future wafers



4 X 4-Bit Static Random Access Memory (RAM)

- Key building block for realizing computational and data storage capability in 500 °C environment
- 220 Transistors
- One 3 X 4-Bit RAM worked on first multilevel interconnect wafer (at room temperature)
 - Design error prevents full 4 x 4-Bit operation
- Mobile ion contamination causes failure of sense amps at elevated temperatures

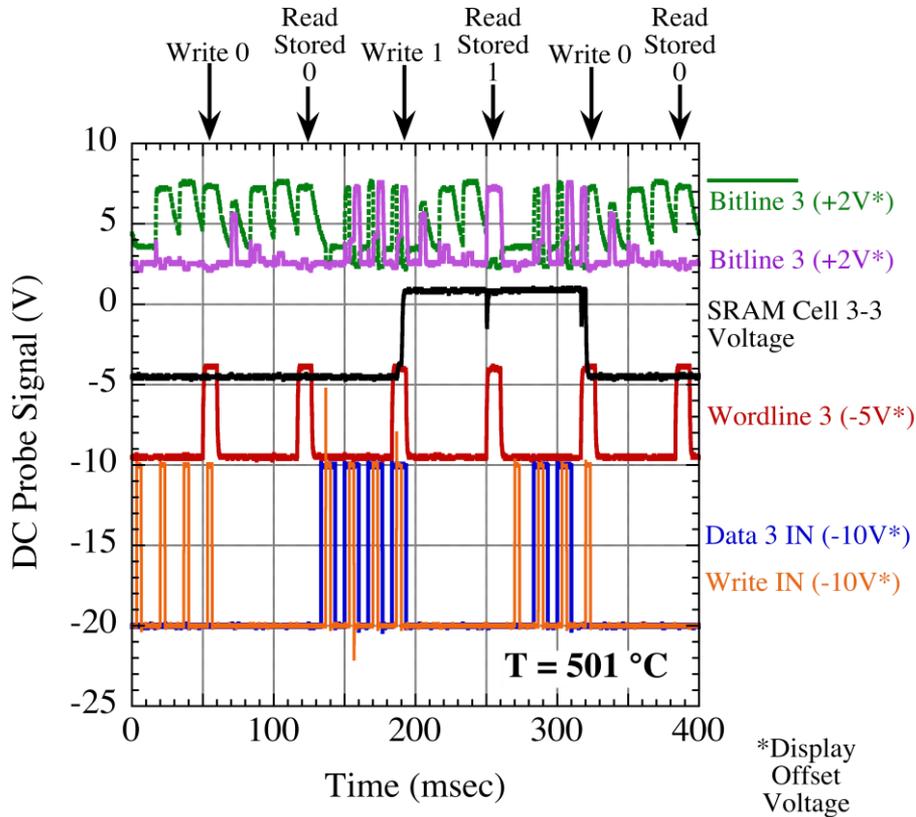


Portion of 4 x 4-Bit RAM

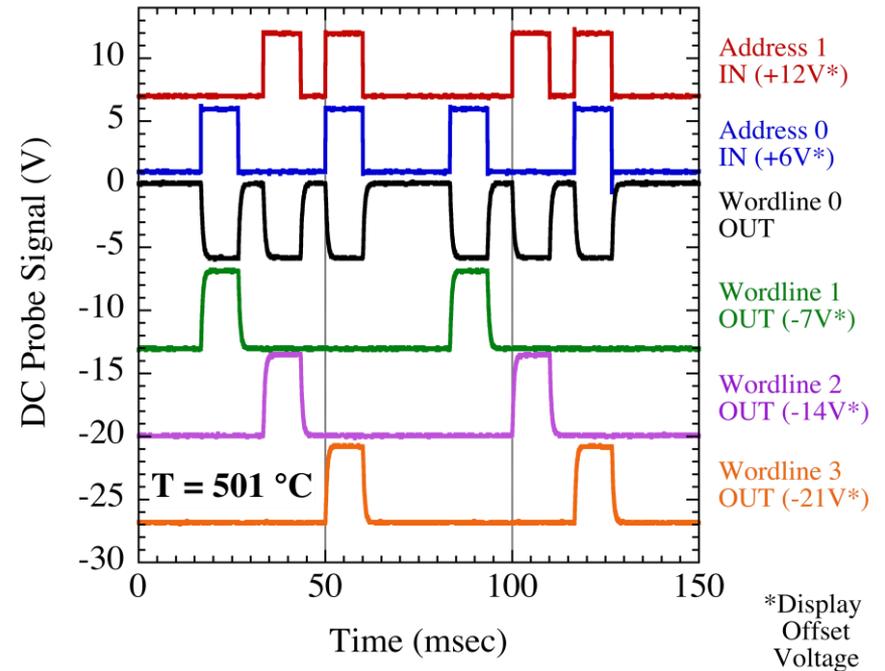


RAM Operation at 500 °C

NASA Glenn SiC RAM Cell 501 °C Test Waveforms



NASA Glenn SiC 4-Bit Address Decoder 501 °C Test Waveforms



Waveforms demonstrate ability to read and write to select bits at 500 °C



Summary

- First demonstration of medium scale integration 500 °C SiC integrated circuits with 10s to 100s of transistors
- Fabrication and test of circuits useful for high temperature smart sensors
 - Ring oscillator – demonstrated 3000 hrs operation at 500 °C
 - D/A - demonstrated at 500 °C (A/D did not work because of design error)
 - RAM - 3 X 4-Bits partly demonstrated at 500 °C (mobile ions prevents sense amps from working at high temperature)
 - Op Amp – demonstrated at room temperature (mobile ions prevent high temperature operation)
- Several significant issues have been uncovered
 - We are working to implement solutions in future wafers
 - Wafer fabrication accelerated
 - Two next generation wafers fabricated within 3 months, room temperature measurements show improved yield.