High Temperature SiC Electronics: Update and Outlook

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Centralized control architecture with FADEC has been used since the mid 1980’s

Distributed engine control features:
- Data concentrators
- Smart sensors/actuators
- Local loop closure
- Digital I/O
- Plug and play
- Sensor bus
- Reduced wire count and weight
- Increased reliability
- Expandability, flexibility, modularity

Implementation of distributed control inhibited by lack of high temperature electronics
- Active cooling of distributed modules is impractical
- Catalog of 225 °C silicon-on-insulator (SOI) electronics needed initially
- Use SiC for T > 300 °C
  - Initially, hot-section applications, e.g., in-combustor smart pressure sensor
  - Longer term, expect higher temperatures more generally
    - Increased power/weight engines
- SiC power electronics for T < 300 °C
Future sensor packages shall incorporate 500 °C SiC amplifiers.

600 °C SiC dynamic pressure sensor installed at station 3.
• Sporian capacitive pressure sensor
• NASA GRC high temperature oscillator circuit
• Cree SiC MESFET (operates at 450°C for over 2 hours)
• Sensor die mounted on circuit board for proof of concept
• Pressurized to 100 psi
• 70% power scavenging to bias electronics
• Transmit distance greater than 1 meter

Initial demo: pressure sensor on circuit board

Prototype (in progress): sensor and circuit packaged for installation in compressor
Wireless Pressure Sensor

Pressure chamber with internal heater for testing wireless pressure sensor circuit board.

Power scavenging assembly – thermoelectric generators operating at 300 ºC and 500 ºC.

Plots show effects of pressure and temperature on signal measured at distance of 1 m.
High Temperature Integrated Circuit Technology

For $T < 150 \, ^\circ\text{C}$, bulk silicon MOSFET (CMOS) is basic building block of almost all (> 95%) integrated circuits in use today (computers, cell phones, etc.).

For $T < 300 \, ^\circ\text{C}$, well-developed Silicon-On-Insulator (SOI) IC’s available for low-power logic and signal processing functions.

Above 300 °C ambient, wide bandgap semiconductors (SiC) are needed.

Many areas of sensing and control interest in jet engines are hotter than 300 °C.

For power electronics: No SOI power electronics. SiC has significant advantages over Si at moderate to elevated temperatures.
Power Applications Drive SiC Development

SiC power electronics cut cooling costs
SiC High Temperature Electronics Technologies

Pursuit of large power device market has funded development of many key technologies useful for SiC high temperature electronics (a niche market).

High temperature specific technologies needed:
• Ohmic contacts
• Integrated circuit design
• Insulators
• Interconnects
• Packaging

500 °C Durable Chip Packaging And Circuit Boards
(L.Y. Chen, 2002 GRC R&T Report)

500 °C Durable Metal-SiC Contacts
(R. Okojie, 2000 GRC R&T Report)
Development of High-Temperature SiC Integrated Circuits

Transistors per IC

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<td>100</td>
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SiC Integrated Circuit Demonstrations:

- Digital NAND, NOR gates
- Analog differential amplifier

- Operational Amplifier
- A/D Converter
- Multiplexer

- Microcontrollers

In-package amplifier for SiC dynamic pressure sensor

Digital electronics for transmission of sensor signals on power cable

- Wireless capacitive pressure sensor
- for propulsion health monitoring (VSST)

Venus seismometer (PIDDP)

Enabling Technologies for SiC Electronics:

- Metal-to-SiC contacts
- High temperature packaging
- SiC transistor (JFET) design

Multilevel Interconnect Structure:
- Conformal metal layers
- High temperature insulating layers

- Increase circuit density
- Increase reliability and yield
- Reduce crystalline defects

~ Apollo Guidance Computer levels of integration (mid 1960’s)

~ First microprocessor levels of integration (Intel 4004, released 1971)
## SiC Electronics Development at NASA Glenn

<table>
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<th>Funding Program</th>
<th>High Temperature SiC Electronics Application</th>
<th>Rationale</th>
<th>Emphasis</th>
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<tr>
<td>VSST</td>
<td>Wireless sensors for propulsion health monitoring</td>
<td>o Energy scavenging ---Fully wireless</td>
<td>RF</td>
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<td>Distributed Engine Control</td>
<td>Wireless sensors for propulsion health monitoring</td>
<td>o Readily retrofit</td>
<td>Digital</td>
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<tr>
<td>Aero Sciences &amp; ERA</td>
<td>Smart sensors and actuators with digital I/O</td>
<td>o First insertion of wireless---Safe</td>
<td>Analog</td>
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<tr>
<td>Department of Energy</td>
<td>In-package amplifier for SiC pressure sensor (for active combustion control)</td>
<td>Reduce cable count</td>
<td>Power</td>
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<td>SiC crystal growth methods for reduced defect densities</td>
<td>o Detect sub psi instabilities</td>
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<td>o Initiate control early</td>
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<td>o Reduced EMI susceptibility</td>
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<td><strong>High level output</strong></td>
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<td></td>
<td></td>
<td>o Increased yield/reliability</td>
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<td></td>
<td>o Large area/high voltage devices</td>
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<td><strong>Reduced defects for</strong></td>
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# SiC ICs Now Being Fabricated

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Inputs</th>
<th>Outputs</th>
<th>Transistors, I/O Pads</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-Bit A/D</td>
<td>Analog voltage signal, optional external clock, output type select</td>
<td>4 bit parallel digital latch, pulse width modulated (PWM)</td>
<td>203 JFETs, 23 I/Os</td>
<td>Internal ring-oscillator clock circuit</td>
</tr>
<tr>
<td>4X4 Bit Static RAM</td>
<td>Read, Write, Data Lines, Address Lines</td>
<td>4 bit parallel digital latch</td>
<td>220 JFETs, 30 I/Os</td>
<td>Address decoder, sense amplifiers</td>
</tr>
<tr>
<td>Source Separation Sensor Signal Transmitter</td>
<td>Capacitive sensor</td>
<td>Frequency modulated with address code</td>
<td>301 JFETs, 20 I/Os</td>
<td>Each sensor signal is tagged with unique address code</td>
</tr>
<tr>
<td>Ring Oscillators</td>
<td>Capacitive sensors</td>
<td>Frequency modulated signals (up to 500 MHz)</td>
<td>10-12 JFETs, 6 I/Os</td>
<td>On-chip large transistors for power amplification</td>
</tr>
<tr>
<td>Binary Amplitude Modulation RF Transmitter</td>
<td>Low power binary signal</td>
<td>High-Power RF signal to antenna</td>
<td></td>
<td>Could connect with PWM from A/D</td>
</tr>
<tr>
<td>Op Amp, 2-Stage</td>
<td>Differential</td>
<td>Voltage gains to 50 w/ on-chip resistors</td>
<td>10 JFETs</td>
<td>For piezoelectric SiC pressure sensors</td>
</tr>
<tr>
<td>4-Bit D/A</td>
<td>4 digital</td>
<td>1 analog</td>
<td>20 JFETs</td>
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SiC High Temperature Electronics Development

In 2007, NASA GRC demonstrated long-term operation of simple SiC analog and digital integrated circuits for at 500 °C.

- Junction field effect transistor (JFET) technology (lateral, n-channel)
  - avoids MOS oxide reliability issues
  - power consumption can limit levels of integration (1 mW per gate)
- Single interconnect layer limits circuit complexity (<10 transistors and resistors per IC)

Since 2007, we have worked to develop more complex medium scale integration (MSI) circuits having 10 to >100 transistors (also large area JFETs).
- High temperature multilevel interconnect structure needed to realize MSI

Simple SiC circuit – NOR gate on probe station

MSI SiC circuit - operational amplifier (early design, partially fabricated)
Single level interconnect (2007)
- 10 µm line width
- Two insulating layers:
  - Thermally grown SiO₂
  - Sputtered Si₃N₄
- Two metal layers
  - Ti/TaSi₂/Pt contacts
  - TaSi₂/Pt interconnect/bondpad

Multilevel interconnect (2013)
- 6 µm line width
- Three insulating layers, deposited by chemical vapor deposition (CVD):
  - Two SiO₂
  - One SiO₂ / Si₃N₄ bilayer
- Three metal layers
  - Ti/TaSi₂ contact/interconnect
  - TaSi₂ interconnect
  - TaSi₂/Pt/Ir/Pt bond pad

Single level interconnect structure (2007)
Multilevel Interconnects to Enable Medium Scale Integration ICs

500 ºC Operation Presents Significant Challenges

A. Step Coverage Issues

- Leakage and breakdown properties of insulating materials are significantly degraded at 500 ºC.
- SiO$_2$ is effective at standing off the voltages of interest, at 1 µm thickness.
- The small feature sizes (6 µm line width) and relatively thick films provide significant surface topography.
- Sputtered metal layers therefore need to cover abrupt steps.
- Typically, step coverage is improved by heating the substrate during the sputter process to a temperature $T$ approaching the melting point $T_m$ of the metal. However this is not feasible with the refractory metals used for high temperature SiC electronics.

B. Thermally Induced Stress

- Metal and oxide have significantly different CTEs
- Cycling from room temperature to 500 ºC (700 – 800 ºC during fabrication) can produce significant stress.
- Affects design of large metal areas (e.g. bond pads).

TaSi$_2$/Pt line delaminates following exposure to 500 ºC, pulling SiO$_2$ from Si wafer.
Conformal Deposition of TaSi2 for 500 ºC Multilevel Interconnects

Close-range sputter deposition process for 3 inch wafers
- 1 inch source-substrate separation
- Film densification by particle bombardment
- Good sidewall coverage
- Substrate rotation and translation provide desired uniformity

Source distance: < Near  Far >

Close range sputtering improves TaSi2 step coverage

NASA designed close-range sputter system
Redesigned Bondpads for High Temperature Integrated Circuits

- The bondpad for the single level interconnect devices was Ti/TaSi$_2$/Pt on sputtered Si$_3$N$_4$ insulator.
- CVD SiO$_2$ has been found to be a superior high temperature insulator and has replaced the sputtered Si$_3$N$_4$ in the MSI wafer.
- However, SiO$_2$ is not as strong and susceptible to cracking as a result of thermally induced stress.
- Therefore, the bond pad has been redesigned so that the metal sits directly on the SiC.
- In addition, a more stable TaSi$_2$/Pt/Ir/Pt bond pad structure is being used.

Photo micrograph of single level interconnect device after prolonged exposure to 500 ºC showing metal degradation.

SEM of bondpads for multilevel interconnect devices.
**MSI SiC Circuit Status**

- One SiC wafer of MSI circuits has been fully processed.
- Circuits were working, with high yield, up until almost the last processing step.
- Deposition of a Si$_3$N$_4$ encapsulating layer was found to introduce many short circuits.
- It was determined that the first metal etch was too short, and left a Ti residue on the surface.
- This residue was oxidized by air to nonconductive TiO$_2$.
- CVD of Si$_3$N$_4$ (800 °C in H$_2$) converted TiO$_2$ back to Ti.
- We were very close to having working MSI circuits!

Following Si$_3$N$_4$ deposition, test structures A and B were found to be shorted.

Cross sectional SEM of parallel TaSi$_2$ lines (A and B) showing short-circuiting Ti residue.
MSI SiC Circuit Status

Some simple circuits and some large area transistors were found to work, demonstrating the effectiveness of our approach for multilevel interconnects.

Below: functional NOR circuit. Right: Pt strip deposited prior to cutting trench using focused ion beam. Below Right: Trench affords view of multilevel interconnect. First and second metal layers are shown.
Summary and Plans for Future Work

- One SiC wafer of MSI circuits has been fully processed.
- We were very close to having working MSI circuits.
- Increasing the duration of the first metal etch by 50% will ensure that the metal is fully cleared from the wafer, with no adverse affects.
- Thermal stresses continue to present a challenge which has motivated design modifications.
- Fabrication of a second wafer is underway. We have completed 3 out of 10 mask steps.
- On successful completion of this wafer we expect to have many 500 °C capable integrated circuits useful for distributed engine control.
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