

INVESTIGATIONS OF NON-MICROPIPE X-RAY IMAGED CRYSTAL DEFECTS IN SiC DEVICES

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ABSTRACT

This paper updates on-going experimental and theoretical investigations of non-micropipe defects imaged by synchrotron white beam X-ray topography (SWBXT) in SiC devices and epitaxial layers. Computer-based thermal modeling of screw-dislocation related breakdown in SiC diodes has been initiated to gain insights into internal temperature profiles as a function of microplasma power. A preliminary study of epitaxial 4H- and 6H-SiC p⁺n mesa diodes indicates that very low angle boundaries, whose electrical properties have not previously been reported, do not significantly impact DC I-V properties (forward and reverse) measured at biases less than 70% of the SiC breakdown field. The presence of very small growth pits on the surface of commercial 4H-SiC epitaxial layers, almost undetectable by high magnification optical microscopy, was revealed by atomic force microscopy and found to correspond to the locations of closed core screw dislocations imaged by SWBXT.

INTRODUCTION

Because of its superior material and electrical properties, silicon carbide (SiC) is expected to enable vastly improved high-power switching devices with substantial benefits to a wide variety of industrial, transportation, and power distribution systems. On a small-scale prototype demonstration basis, the high voltage, high current density, and high switching speed capability of SiC continues to improve even though it already well exceeds the theoretical limits of silicon power switching devices. However, SiC power switching devices have yet to be commercialized. This is largely due to SiC crystal defects, most notably the device-killing micropipe defect, which does not permit large-area (i.e., high total current) SiC parts to be realized with sufficiently high manufacturing yields. Great progress towards eliminating this technological obstacle has been made by reducing SiC micropipe densities from several hundreds per square cm in 1993 to less than 1 per square cm in 1998 in the best reported wafers [1]. This could enable micropipe-free power devices on the order of 1 cm² area rated for 100's of amps on-state current to become feasible in the near term.

Unfortunately however, present-day commercial SiC wafers and epilayers contain an abundance of non-micropipe crystal defects, which by and large are best observed on a non-destructive basis by SWBXT. Closed core screw dislocations are found in all commercial wafers in densities of thousands per square cm [2]. Therefore, virtually all multi-amp SiC high voltage devices manufactured in the near term seem guaranteed to contain these defects. It is therefore crucial to understand the impact of non-micropipe defects on various SiC device structures,

particularly high power device structures that will be subjected the harshest electrical and thermal operational stresses.

PN JUNCTION DIODES - THERMAL MODELING

While not nearly as detrimental to high-field device characteristics as micropipes, recent studies have shown that local SiC pn junction electrical properties are measurably altered at closed core screw dislocations. Detailed studies of low-voltage (< 250 V) 4H-SiC p^+n diodes found that closed core screw dislocations were responsible for increased reverse leakage and localized microplasmic breakdown at electric fields slightly below the defect-free junction breakdown field [3, 4]. The microplasma power, which appeared to be limited by space-charge effects and the relatively low operating voltages of these diodes, was not sufficient to damage these devices, even when pulse-breakdown tested at power densities as high as megawatts per square cm [5]. However, quantitative values for peak junction temperature and temperature coefficient of breakdown voltage could not be directly extracted from these measurements.

Computer-based thermal modeling of 4H-SiC mesa diodes has been initiated in an effort to estimate internal device temperature profiles during various breakdown testing conditions. Two-dimensional (2D) and three-dimensional (3D) simulations on a $100\ \mu\text{m}$ diameter circular mesa diode structure (depicted in Figure 1) etched on top of a $1\ \text{mm} \times 1\ \text{mm} \times 0.3\ \text{mm}$ 4H-SiC chip (not shown in Figure 1) were performed using commercial thermal modeling software [6]. The

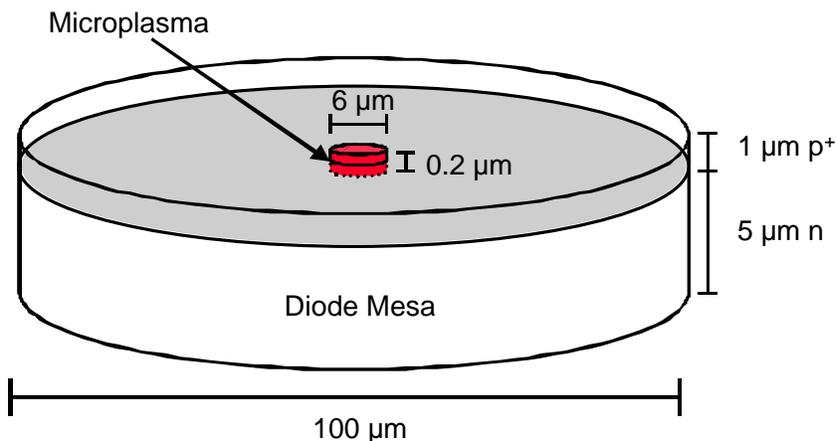


Figure 1: Schematic depiction of simulated microplasma heat generation region in the center of SiC pn diode mesa (see text).

bottom of the $1\ \text{mm} \times 1\ \text{mm} \times 0.3\ \text{mm}$ chip was set as an infinite heat sink to room temperature (293 K), while convective heat transfer with air at room temperature was assumed for the remaining surfaces of the structure. Temperature dependent thermal conductivity and heat capacity reported in [7] were employed in the simulations. All heating was assumed to occur within a $0.2\ \mu\text{m}$ thick layer at the metallurgical

pn junction where the electric field profile is at its maximum. This assumed layer thickness is smaller than junction breakdown depletion widths for SiC diodes doped less than $10^{18}\ \text{cm}^{-3}$. The lateral diameter of microplasmas optically observed in [4] was about $6\ \mu\text{m}$. Therefore, a microplasma was approximated in 3D simulations as a uniformly heated cylinder $0.2\ \mu\text{m}$ tall with $6\ \mu\text{m}$ diameter at the metallurgical pn junction in the center of the diode mesa (Figure 1). Taking a 2D planar slice down through the middle of the cylinder gives a $6\ \mu\text{m} \times 0.2\ \mu\text{m}$ box for 2D simulations. Total microplasma power for the 2D simulations was approximated by extending the 2D box $6\ \mu\text{m}$ into the third dimension. Because heat energy flows out of the hot microplasma into the cooler semiconductor in all dimensional directions, the 3D simulations

Table I: Peak temperatures calculated for various microplasma powers.

Simulation	Microplasma Power	Peak Temperature
2D	0.1 W	421 K
3D	0.1 W	323 K
2D	0.25 W	774 K
3D	0.91 W	778 K
2D	0.35 W	1274 K
3D	1.3 W	1276 K
2D	0.41 W	1773 K
3D	1.5 W	1773 K

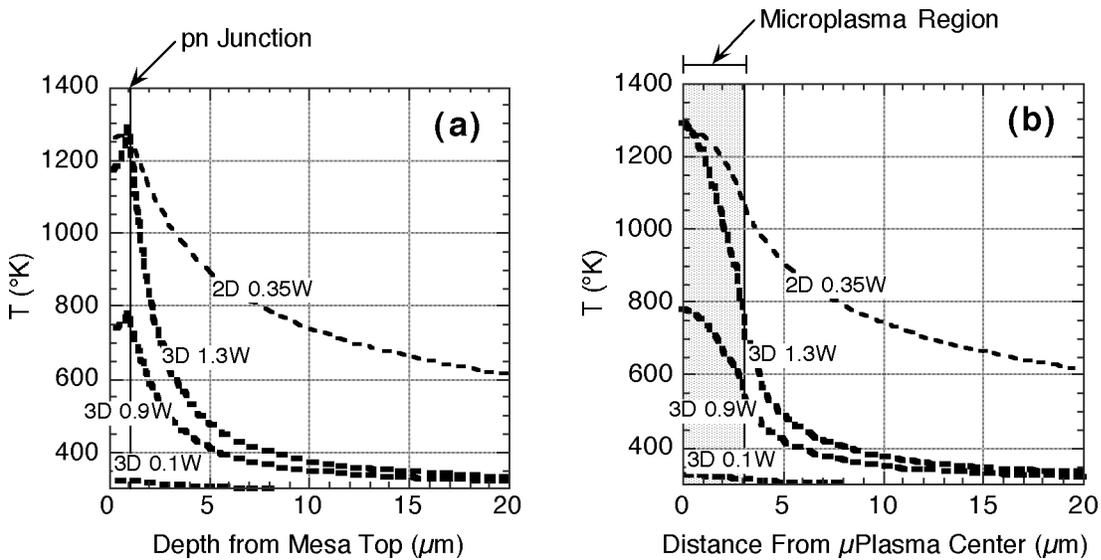


Figure 2: Calculated temperature profiles for selected microplasma input powers. (a) Temperature as a function of vertical depth from the top surface along the vertical centerline of the microplasma. (b) Temperature as a function of radial horizontal distance from the microplasma center along the metallurgical pn junction.

should give more accurate results than 2D simulations in which energy flow is, in a less accurate physical approximation of the microplasma, restricted to two dimensional directions. Nevertheless, quantitative understanding of the temperature profile differences between 2D and 3D simulations is important, since not all electrothermal device modeling software is 3D-capable.

The peak temperatures obtained at the center of the microplasma in DC simulations are summarized in Table I. Placing a total DC microplasma power of 0.1 W within the 0.2 μm tall cylinder, which is close to the microplasma powers experimentally measured in [4], the 3D simulation estimates a peak temperature of 323 K at the center of the microplasma. This temperature is clearly not sufficient to cause device damage, which is consistent with experimental observations in [3, 4]. As expected, the 2D simulations yield higher peak temperatures than 3D simulations at comparable input powers, or alternatively, lower input

powers to reach a comparable temperature as the 3D simulations, due to loss of heat flow in the third dimension. Other DC thermal simulations listed in Table I illustrate microplasma power densities that would be necessary to reach peak temperatures around 773 K (500 °C), 1273 K (1000 °C), and 1773 K (1500 °C). Figure 2 illustrates the simulated temperature profiles extending from the vertical and lateral microplasma centerlines for the 3D 0.1 W, 0.91 W, and 1.3 W input power cases as well as the 2D 0.35 W input power case. The calculated temperature (~ 1150 K) reaching the top contact in the 3D 1.3 W microplasma simulation in Figure 2(a) could cause contact degradation over time and/or repeated exposure to localized breakdown. While not directly addressed in this work, it should be noted that SiC Schottky diodes are expected to fail at lower local heating temperatures than SiC pn junctions, in large part due to the fact that SiC Schottky leakage currents grow large with increasing temperature above 500 °C. Alternative device packaging geometries which promote heat removal through the top contact could beneficially reduce peak temperatures within the device at a given microplasma power density.

Though apparently not an important factor for lower voltage SiC devices, the impact of closed core screw dislocations and localized breakdown on the avalanche rating and safe operating area of high voltage devices remains to be investigated. As discussed by Chynoweth [8], previous microplasma theory and experience indicates that reverse bias microplasma currents fall within an order of magnitude of 0.1 mA in almost all semiconductors, and the microplasma current is relatively insensitive to junction width and doping (i.e., junction breakdown voltage). The ~ 0.1 – 1 mA nondestructive microplasma currents reported to date in reverse-biased 4H-SiC pn junctions appear quite consistent with this model [3, 4, 9, 10]. Therefore, it is conceivable that the power density of localized 4H-SiC current filaments may greatly increase as SiC device blocking voltage is increased to 1 kV or 10 kV envisioned for many high-power applications. A most pessimistic worst-case assumption would be that the microplasma current and current density does not drop at all as the device blocking voltage is increased, so that the power density would directly increase with blocking voltage. Under the worst-case assumption where microplasma diameter remains 6 μm, microplasma thickness remains 0.2 μm, and microplasma current remains 1 mA as diode blocking voltage is increased, blocking voltages of 1.3 kV and 1.5 kV would correspond to the 1276 K and 1773 K peak microplasma temperatures, respectively, as calculated in Table I. Neglecting the effects that high microplasma temperatures have on device contacts and surface passivation, these worst-case calculations indicate that microplasmas in closed core screw dislocations should not cause destructive DC breakdown testing failures (at least in the short term) in SiC pn junctions rated below ~ 1 kV. This is consistent with the fact that experimental reports of non-destructive DC microplasmas in the SiC literature to date have been confined to pn junctions of less than 600 V blocking capability [3, 4, 9, 10].

While understanding of DC behavior is an important first step, most electrothermal stresses encountered by devices in fielded power circuits are transient in nature, usually brief duration single-event “fault” stresses or repetitive-event “switching” stresses. Transient electrothermal modeling is necessary to further understand current and heat distributions in devices subjected to various short-duration stress conditions in circuits. Efforts are underway to model the pulse-breakdown behavior, with and without microplasmas, of the mesa diode structure of Figure 1 and Ref. [5].

PN DIODE CHARACTERIZATION

Some of the discussion in the preceding section was based upon worst-case assumptions regarding the physical behavior of closed core screw dislocations and microplasmas. Quantitative verification of predicted behaviors in experimental high-voltage junctions is obviously an important next step in the process of further understanding of closed core screw dislocation behavior in SiC devices. Towards that end, an experiment was undertaken to map and characterize X-ray imaged defects in higher voltage 4H- and 6H-SiC pn junction diodes.

4H and 6H mesa etched diodes with doping cross-sections shown in Figure 3 were epitaxially grown and processed side-by-side into devices at NASA Glenn Research Center. Patterned mesas were RIE etched to a depth of 5 μm using liftoff-patterned indium tin oxide as an etch mask. The etch mask was then stripped, and mesa isolation electrically verified using a curve-tracer probing the p^+ SiC contact epilayer. Nickel was then

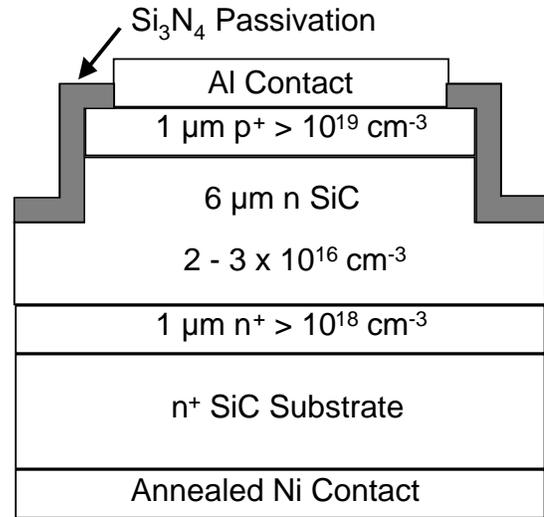


Figure 3. Cross-section of experimental 4H- and 6H-SiC pn junction diodes.

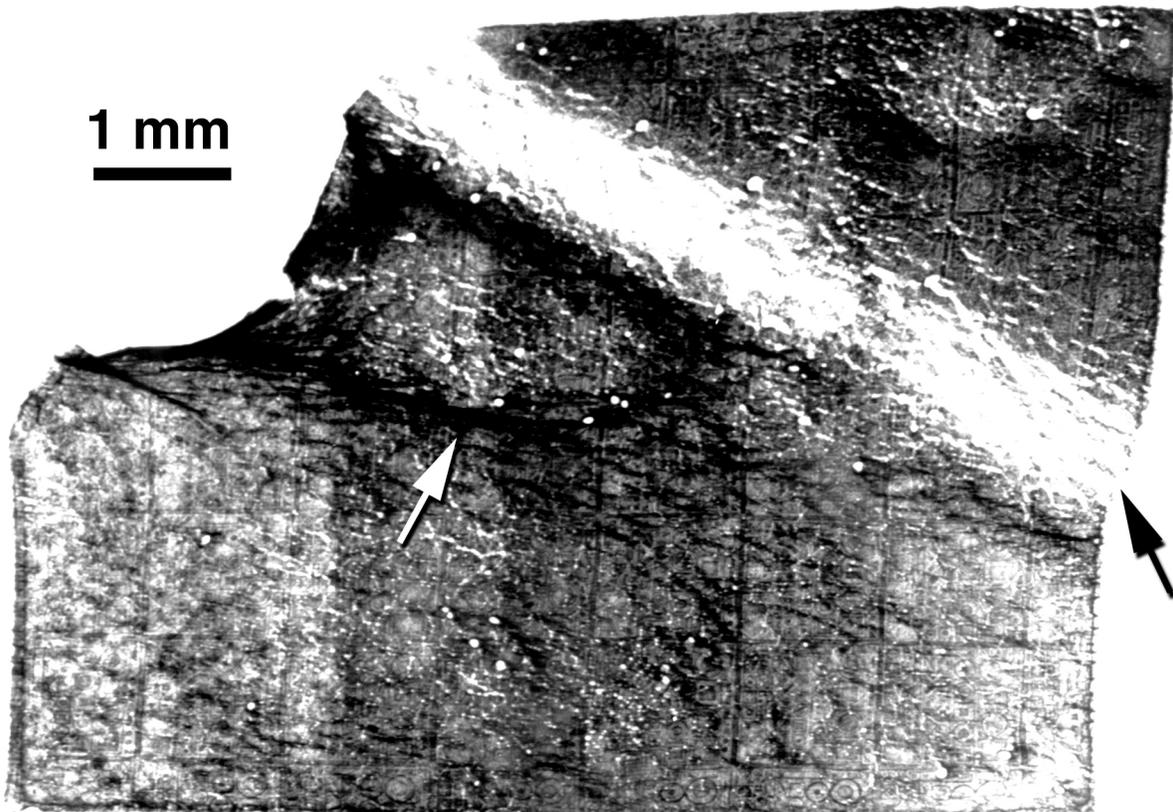


Figure 4: Back-reflection topograph of 6H-SiC pn junction diode wafer piece. The arrows point to examples of small-angle boundary features in the topograph.

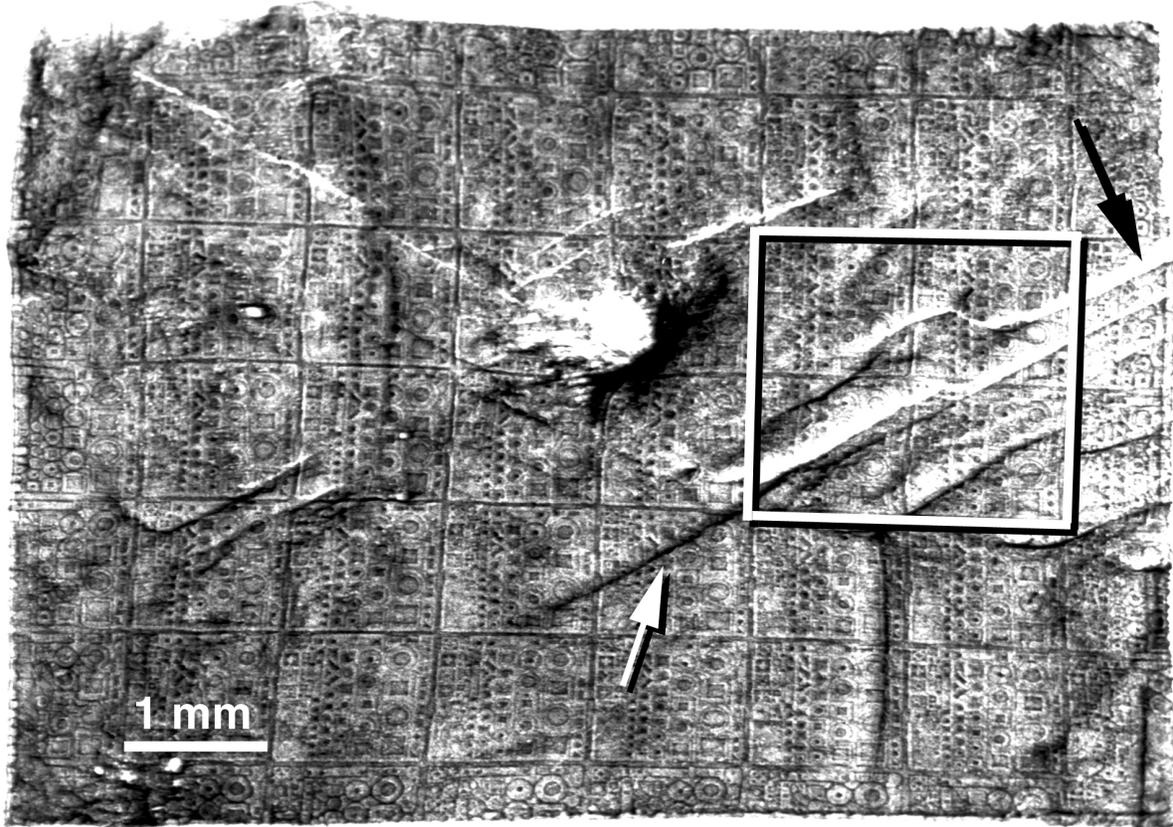


Figure 5: Back-reflection topograph of 4H-SiC pn junction diode wafer piece. The arrows point to examples of small-angle boundaries in the topograph.

deposited and annealed at 900 °C for 5 minutes in an argon tube furnace to make a backside ohmic contact to the wafer. A passivation layer of silicon nitride was then deposited by plasma CVD and via holes etched. The wafers were then back-reflection imaged by SWBXT. Aluminum topside contacts were then E-beam deposited and patterned by liftoff.

Figures 4 and 5 show the back-reflection X-ray topographs of the 6H-SiC and 4H-SiC pn diode wafers, respectively. While some individual closed core screw dislocations were resolvable, the SWBXT images were not quite sufficient to enable clear resolution of most closed core screw dislocations on the wafers, especially in the 4H sample. The presence of annealed back contact metal, non-polished backside, and Si₃N₄ passivation on the sample is believed responsible for the somewhat degraded image quality. With this difficulty, small-angle boundaries that image as somewhat linear light and dark regions became the first focus of the study on these samples. The electrical properties of these defects in SiC has not previously been reported. The crystal lattice on one side of a small-angle boundary is slightly tilted with respect to the lattice on the other side of the boundary. In back-reflection X-ray topography, the boundaries are visible via "orientation contrast" whereby the diffracted beams emanating from either side of the boundary either converge leading to overlap on the image (dark contrast) or diverge leading to separation (light contrast). The relative tilt angles involved in the boundaries shown in the Figure 4 and 5 images are on the order of a few arc minutes or less.

Device forward and reverse I-V properties were characterized on a probing station in near-dark conditions. Even though the devices were designed for ~ 1 kV blocking and tested in

Fluorinert to prevent arcing, undesired destructive edge failure limited the reverse breakdown voltage to less than 500 V typically. This shortcoming limited reverse measurements to electric fields of less than 70% of the published SiC breakdown field. Given that non-micropipe microplasma formation is reported to occur at greater than 80% of the bulk SiC breakdown field in lower-voltage devices, the edge failures did not permit direct observation of microplasmas at closed core screw dislocations in a similar manner as reported in [3, 4]. Edge-related failures (often destructive) are a common problem that often limit the blocking voltage performance of most reported SiC high voltage (i.e., > 1 kV) diodes, thereby hindering the observation of bulk and dislocation assisted breakdown phenomenon. If silicon power device reliability experience holds for SiC, improvement of high-voltage SiC diode edge terminations to permit bulk avalanche breakdown and large safe operating area will be an important step towards the realization of higher reliability SiC power devices.

Figures 6 and 7 illustrate representative data generally consistent with I-V mapping carried out on over 100 devices on both wafer pieces. In particular, forward and reverse I-V data collected on 150 μm circular (diameter) and square (side) 4H-SiC pn junction devices within the region highlighted by the box in Figure 5 are used for illustration. The I-V curves plotted with thin solid lines represent devices with no light or dark small-angle boundary features in the topograph. The I-V curves plotted with thick solid and dashed lines were recorded from devices with large dark or light small-angle boundary features, respectively, clearly intersecting them in the topograph.

The forward I-V's in Figure 6 show well-behaved exponential turn-on with ideality factors very close to two in all cases, indicating recombination as the dominant current conduction mechanism [11]. This characteristic was consistently observed in the vast majority of devices on both wafers, even in devices that X-ray showed to contain a closed core screw dislocation. This finding suggests that closed core screw dislocations by themselves are not responsible for large anomalous "bumps" in exponential forward I-V characteristics of SiC pn junction diodes [12]. For forward biases above 3 V, the region of the I-V usually dominated by device series resistance, there is an unexpectedly large scatter in current that does not appear to scale with any

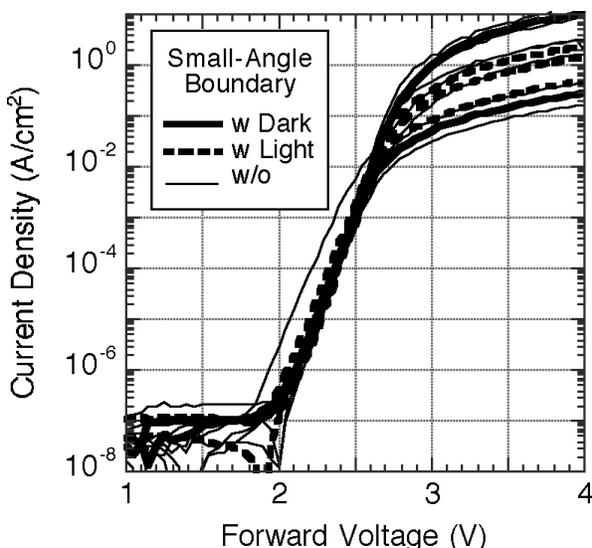


Figure 6: Forward I-V characteristics of 150 μm sized devices in boxed region of Figure 5 (see text).

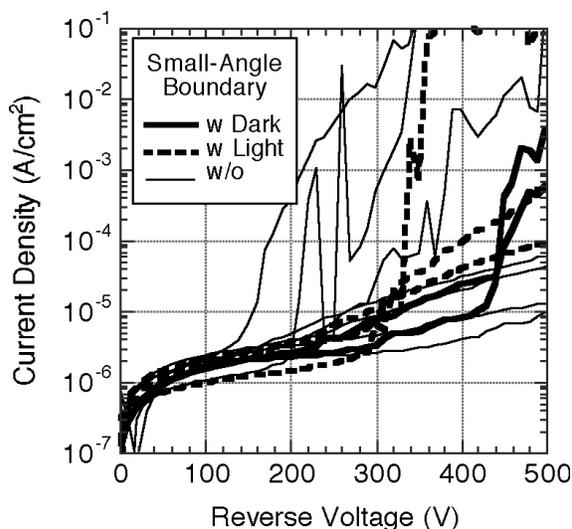


Figure 7: Reverse I-V characteristics of 150 μm sized devices in boxed region of Figure 5 (see text).

readily observable device property such as contact area, mesa area, perimeter-to-area ratio, general mesa location on the wafer, or presence of observable X-ray imaged stress region. It is possible that unmeasured variations in non-optimized ohmic contact properties contribute to the large series resistance scatter.

Figure 7 shows the corresponding reverse I-V's recorded with the devices immersed in Fluorinert. The dependence of leakage current as a function of the device residing in an X-ray imaged small-angle boundary is mostly inconclusive. The best (i.e., lowest leakage current) devices near 500 V in Figure 7 are free of small-angle boundary features, but not all devices off the small-angle boundaries are good. Similarly, measurements on devices on and off the small-angle boundary of Figure 4 also lack any readily observable trends. Edge-leakage and unresolved defects may be interfering factors producing scatter in leakage currents at higher voltages. As is the case with closed core screw dislocations [4], higher electric fields (i.e., greater than 80% of the defect-free critical field) may be required before significant differences in device I-V properties due to small-angle boundaries can be readily observed. However at the electric fields employed in this study, the X-ray imaged small-angle boundaries did not significantly impact either forward or reverse I-V characteristics of these 4H- and 6H-SiC pn junction diodes.

EPI-LAYER SURFACE CHARACTERIZATION

Schnabel et al. recently reported a simultaneous study of 6H-SiC Schottky diodes (epilayers grown by CVD at NASA Glenn starting from 3.5° off-axis commercial wafers) by Electron Beam Induced Current (EBIC), SWBXT, Nomarski optical microscopy, and Atomic Force Microscopy (AFM) [13]. It was found that closed core screw dislocations corresponded to both a local decrease in EBIC-measured minority carrier lifetime as well as the presence of sharp-tipped very small growth pits in the epilayer surface.

A similar study on commercially purchased 6H-SiC (3.5° off-axis, Sample A) and 4H-SiC (8° off-axis Sample B and Sample C) epilayers has been undertaken. Samples A and B have $9\ \mu\text{m}$ thick “standard” (manufacturer’s specification [14]) epilayers that were produced side-by-side during the same epitaxial growth run. Very small growth pits, very difficult to observe even

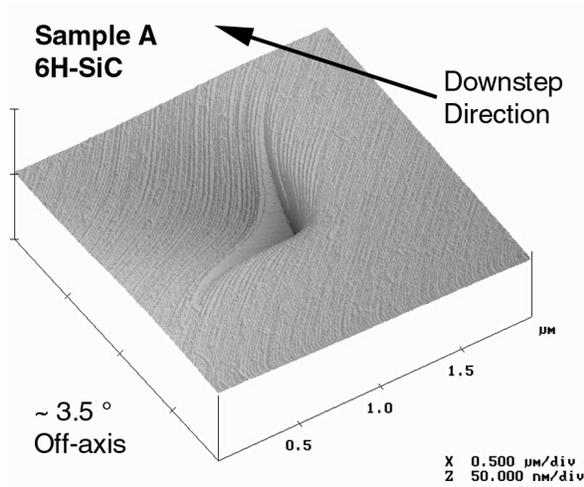


Figure 8: AFM of sharp tip of very small growth pit feature on $9\ \mu\text{m}$ thick 6H-SiC commercial epilayer (Sample A).

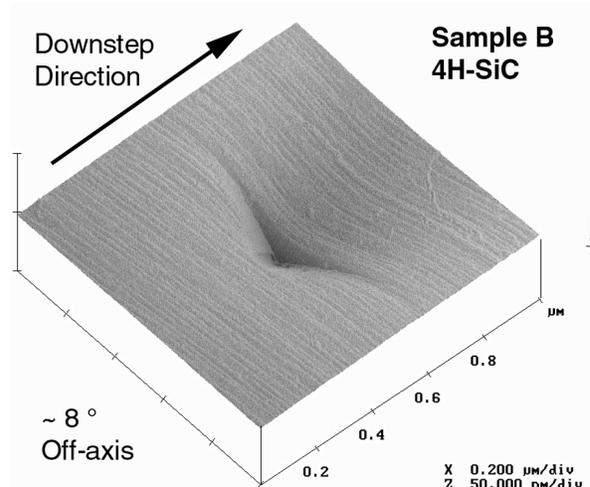


Figure 9: AFM of sharp tip of very small growth pit feature on $9\ \mu\text{m}$ thick 4H-SiC commercial epilayer (Sample B).

using high-quality 400X Nomarski optical microscopy, were detected and subsequently analyzed by AFM. AFM images comparing the pits on the Samples A and B are shown in Figures 8 and 9, respectively. The images are of sufficient quality that the off-axis surface step structure is clearly evident. The head of the pit in both samples appears to originate from a very localized impediment to the lateral flow of surface steps that occurs during off-axis step-controlled homoepitaxy of SiC. With stepflow partially impeded at a sharp point, a small “wake” results “downstream” (i.e., in the downstep direction) that appears to expose an appreciable portion of a (0001) basal plane in both pits. The size of the exposed plane in 6H Sample A is over twice that of the exposed plane in 4H Sample B, consistent with the more than two-fold difference in off-axis polish angle of the two samples. The measured depths of the sharp tip of the pits on 6H-SiC Sample A and 4H-SiC Sample B are approximately 19 nm and 15 nm, respectively. Similarly, the shallower gradual depressions (i.e., the shallow “wake” “downstream” of the exposed basal plane) are noticeably longer on the 6H sample (~ 3-4 μm) than on the 4H sample (~ 1-2 μm). Given the very small sizes (in the X-Y plane) of the sharp tips, the larger gradual depressions are believed to be what is actually detected when observing the sample by high-magnification Nomarski optical microscopy.

4H-SiC Sample C, which has a 10 μm thick standard commercial epilayer [14], was specially prepared for accurate spatial mapping of closed-core screw dislocations by dry etching a patterned registration grid of die borders into the sample and polishing the wafer backside prior to SWBXT imaging. The

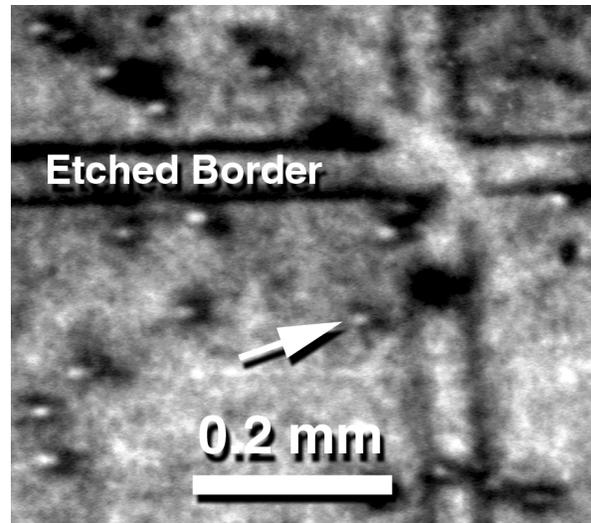


Figure 10: Back-reflection SWBXT enlargement of 4H-SiC epitaxial wafer section (Sample C) featuring closed core screw dislocations (light dot features) and die borders into the surface.

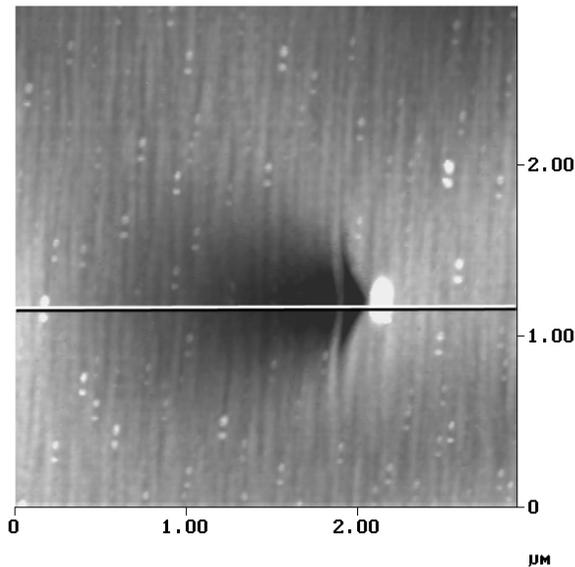


Figure 11: AFM scan of very small growth pit defect on 4H-SiC Sample C. The location of this pit corresponds to the location of the closed core screw dislocation highlighted by the Figure 10 arrow.

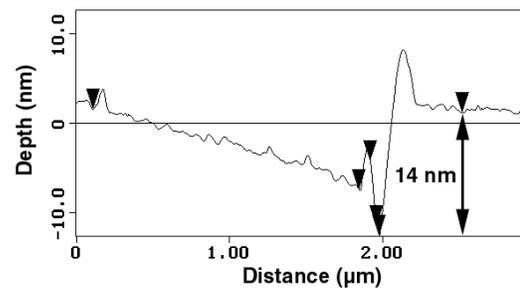


Figure 12: AFM depth profile of very small growth pit defect on Sample C taken across line shown in Figure 11 AFM image.

registration etch was carried out by liftoff-patterning a nickel mask and inductively coupled plasma etching to a depth of nearly 10 μm . The etch mask was stripped and the wafer chemically cleaned before X-ray imaging. As shown in the X-ray topographic enlargement of Figure 10, both etched die borders and individual closed-core screw dislocations (light dot features) are observable.

Figure 11 shows an AFM enlargement of a very small growth pit defect found in Sample C where SWBXT imaging indicates there is a closed core screw dislocation. This particular screw dislocation is denoted by the white arrow in Figure 10. Figure 12 illustrates the AFM-measured depth profile along the white line denoted in Figure 11. The pit is nearly identical in size, appearance, and depth (14 nm) with the very small growth pit measured on 4H-SiC Sample B (Figure 9). To date, five other growth pits nearly identical to Figure 11 have been documented on Sample C where X-ray imaging indicates the presence of a corresponding closed core screw dislocation. The basic nature of these very small pits is consistent with a formation mechanism in which stepflow during epitaxial growth is partially impeded by the presence of the closed core screw dislocation. AFM scans conducted on material away from the pits has thus far failed to locate surface features with similar characteristics.

It is important to note that observation of these growth pits by optical Nomarski microscopy, even at 400X and 1000X magnifications, was exceedingly difficult. The sharp-tipped pits were often camouflaged by the presence of small particles, larger epilayer growth pits, and the replication of polishing scratches on the epilayer surface. Thus it is not surprising that these growth pits features are not accounted for in the epiwafer manufacturer's specification, in which optical inspection is limited to 200X magnification [14]. The very small epilayer growth pits reported here are clearly smaller and of a noticeably different nature than previously reported epilayer growth pits [15]. The specific impact of both these growth pit features on the performance and reliability of various surface-sensitive device structures such as MOSFET's and Schottky diodes remains to be investigated.

SUMMARY

Updated data from ongoing investigations into the nature and electrical impact of stress-inducing X-ray imaged crystal defects has been presented. Thermal modeling studies suggest that localized reverse breakdown microplasmas arising at closed core screw dislocations should not destructively fail SiC pn junction diodes until blocking voltages exceed ~ 1 kV. Large low-angle boundary stress features revealed by X-ray topographic mapping did not significantly impact the DC I-V properties of pn junctions operated at less than 70% of the SiC breakdown field. Very small, sharp-tipped pits in as-grown commercial 4H-SiC epilayer surfaces have been characterized by AFM. Preliminary studies indicate these pits correspond to the locations of closed core screw dislocations mapped by SWBXT.

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